WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, comprising the steps of:

forming a gate electrode on a semiconductor substrate;

forming low concentration impurity regions by performing ion implantation on said semiconductor substrate by using said gate electrode as a mask;

depositing a first insulating film over said semiconductor substrate in which said low concentration impurity regions are formed;

forming first sidewall insulating films on the side surfaces of said gate electrode by performing anisotropic dry etching on said first insulating film;

forming high concentration impurity regions by performing ion implantation on said semiconductor substrate by using said gate electrode and said first sidewall insulating films as a mask;

depositing a second insulating film over said semiconductor substrate in which said high concentration impurity regions are formed;

forming second sidewall insulating films on the portions of said high concentration impurity regions located in proximity to said low concentration impurity regions and on the side surfaces of said first sidewall insulating films by performing anisotropic dry etching on said second insulating film; and

selectively forming metal silicide layers on the exposed region of each surface of said semiconductor substrate and said gate electrode by using said first sidewall insulating films and said second sidewall insulating films as a mask.

2. The method for manufacturing a semiconductor device according to claim 1, further comprising a step of:

performing ion implantation on said semiconductor substrate by using said gate electrode, said first sidewall insulating films, and said second sidewall insulating films as a mask, in between the step of forming said second sidewall insulating films and the step of forming said metal silicide layers, making the depth of said high concentration impurity

regions except for their portions located underneath said second sidewall insulating films deeper than the depth of these portions located underneath said second sidewall insulating films in said high concentration impurity regions.

3. The method for manufacturing a semiconductor device according to claim 1, further comprising a step of:

forming a resist pattern to cover the portion of said second insulating film deposited on the top side of a resistance element-forming region in said high concentration impurity region, in between the step of depositing said second insulating film and the step of forming said second sidewall insulating films; and wherein:

the step of forming said second sidewall insulating films includes a step of performing anisotropic dry etching on said second insulating film by using said resist pattern as a mask to leave said second insulating film on said resistance element-forming region.

4. The method for manufacturing a semiconductor device according to claim 1, further comprising a step of:

forming offset spacers on the side surfaces of said gate electrode in between the step of forming said gate electrode and the step of forming said low concentration impurity regions; and wherein:

the step of forming said low concentration impurity regions includes a step of performing ion implantation on said semiconductor substrate by using said gate electrode and said offset spacers as a mask to form said low concentration impurity regions.

5. A method for manufacturing a semiconductor device, comprising the steps of:

partitioning a first transistor-forming region and a second transistor-forming region by forming an isolation insulating film in a semiconductor substrate;

forming a first gate electrode on said first transistor-forming region with a first gate insulating film interposed between the first gate electrode and the first transistor-forming region;

forming a second gate electrode on said second transistor-forming region with a second gate insulating film interposed between the second gate electrode and said second transistor-forming region;

forming first low concentration impurity regions by performing ion implantation on said first transistor-forming region by using said first gate electrode as a mask;

forming second low concentration impurity regions by performing ion implantation on said second transistor-forming region by using said second gate electrode as a mask;

depositing a first insulating film over the semiconductor substrate in which said first low concentration impurity regions and said second low concentration impurity regions have been provided;

forming first sidewall insulating films on the side surfaces of said first gate electrode and, at the same time, forming second sidewall insulating films on the side surfaces of said second gate electrode, by performing anisotropic dry etching on said first insulating film;

forming first high concentration impurity regions by performing ion implantation on said first transistor-forming region by using said first gate electrode and said first sidewall insulating films as a mask;

forming second high concentration impurity regions by performing ion implantation on said second transistor-forming region by using said second gate electrode and said second sidewall insulating films as a mask;

depositing a second insulating film over said semiconductor substrate in which said first high concentration impurity regions and said second high concentration impurity regions have been formed;

forming third sidewall insulating films on the portions of said second high concentration impurity regions located in proximity of said second low concentration impurity regions and on the side surfaces of said second sidewall insulating films, by performing anisotropic dry etching on said second insulating film; and

selectively forming metal silicide layers on the exposed region of each surface of said first transistor-forming region, said second transistor-forming region, said first gate electrode, and said second gate electrode by using said isolation insulating films, said first sidewall insulating films, said second sidewall insulating films, and said third sidewall insulating films as a mask.

6. The method for manufacturing a semiconductor device according to claim 5, wherein;

the step of forming said third sidewall insulating films includes a step of forming fourth sidewall insulating films on the portions of said first high concentration impurity regions located in proximity of said first low concentration impurity regions and on the side surfaces of said first sidewall insulating films: and further comprising the step of;

selectively removing said fourth sidewall insulating films by using a resist pattern covering said second transistor-forming region as a mask, and thereafter removing said resist pattern, in between the step of forming said third sidewall insulating films and the step of forming said metal silicide layers.

7. The method for manufacturing a semiconductor device according to claim 5, wherein;

the step of forming said third sidewall insulating films includes a step of forming said third sidewall insulating films by performing anisotropic dry etching on said second insulating film by using a first resist pattern covering said first transistor-forming region as a mask, and thereafter removing said first resist pattern: and further comprising a step of;

selectively removing the residual portion of said second insulating film remaining on said first transistor-forming region by using a second resist pattern covering said second transistor-forming region as a mask, and thereafter removing said second resist pattern, in between the step of forming said third sidewall insulating films and the step of forming said metal silicide layers.

8. The method for manufacturing a semiconductor device according to claim 7, wherein:

said first resist pattern is formed to cover the portion of said second insulating film lying on the top side of a resistance element-forming region in said second high concentration impurity region; and

the step of forming said third sidewall insulating films includes a step of leaving said second insulating film on said resistance element-forming region.

9. The method for manufacturing a semiconductor device according to claim 5, further comprising a step of:

performing ion implantation on said second transistor-forming region by using the resist pattern covering said first transistor-forming region, said second gate electrode, said second sidewall insulating films, and said third sidewall insulating films as a mask, making the depth of said second high concentration impurity regions except for their portions located underneath said third sidewall insulating films deeper than the depth of these portions located underneath said third sidewall insulating films in said second high concentration impurity regions, in between the step of forming said third sidewall insulating films and the step of forming said metal silicide layers.

10. A semiconductor device comprising a MIS transistor having:

a gate insulating film formed on a transistor-forming region in a semiconductor substrate;

a gate electrode formed on said gate insulating film;

first sidewall insulating films formed on the side surfaces of said gate electrode;

low concentration impurity regions formed underneath said first sidewall insulating films in said transistor-forming region; and

high concentration impurity regions formed outside said gate electrode in said transistor-forming region so as to adjoin to said low concentration impurity regions; wherein:

second sidewall insulating films are formed on the portions of said high concentration impurity regions located in proximity to said low concentration impurity regions and on the side surfaces of said first sidewall insulating films; and

metal silicide layers are formed on the surface of said gate electrode and on the surfaces of said high concentration impurity regions except for their portions located underneath said second sidewall insulating films.

11. The semiconductor device according to claim 10, wherein:

said metal silicide layer is discontinuously provided on the surface of said high concentration impurity region except for its portion located underneath said second sidewall insulating film.

12. The semiconductor device according to claim 10, wherein:

the depth of said high concentration impurity regions except for their portions located underneath said second sidewall insulating films are deeper than the depth of the portions of said high concentration impurity regions located underneath said second sidewall insulating films.

13. The semiconductor device according to claim 10, further comprising another MIS transistor having:

another gate insulating film formed on another transistor-forming region in said semiconductor substrate and having a thickness thinner than said gate insulating film;

another gate electrode formed on said another gate insulating film;

another sidewall insulating films formed on the side surfaces of said another gate electrode;

another low concentration impurity regions formed underneath said another sidewall insulating films in said another transistor-forming region; and

another high concentration impurity regions formed outside said another gate electrode in said another transistor-forming region so as to adjoin to said another low concentration impurity regions; wherein:

another metal silicide layers are formed on each surface of said another gate electrode and said another high concentration impurity regions.